# The Micro-Isolation Valve Concept: Initial Results of a Feasibility Study

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**A feasibility investigation for a newly proposed microfabricated, normally-closed isolation valve was initiated. The micro-isolation valve is silicon based and relies on the principle of melting a silicon plug, opening an otherwise sealed flow passage. This valve may thus serve a similar role as a conventional pyrovalve and is intended for use in micropropulsion systems onboard future microspacecraft, having wet masses of no more than 10-20 kg, as well as in larger scale propulsion systems having only low flow rate requirements, such as ion propulsion or Hall thruster systems. Two key feasibility issues - melting of the plug and pressure handling capability - were addressed. Thermal finite element modeling showed that valves with plugs having widths between 10 and 50 μm have power requirements of only 10 - 30 Watts to open over a duration of 0.5 ms or less. Valve chips featuring 50 micron plugs were burst pressure tested and reached maximum pressure values of 2900 psig (19.7 Mpa).**

micro valve
MEMS
MEMS-valve

## I. INTRODUCTION

There currently exists a strong interest within the aerospace community to built ever smaller spacecraft to reduce the costs of space missions and afford more frequent launches. Most recently, this trend towards smaller and lighter spacecraft has accelerated as demonstrated by the introduction of the concept of the microspacecraft, typically understood as a spacecraft in the 10-kg class or less, as pursued by the National Aeronautics and Space Administration (NASA)[1], for example. Such dramatic decreases in spacecraft weight and size and, associated with the former, available power levels possibly exceeding not exceeding a few tens of Watts, will require radically new approaches in the design of spacecraft components.

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An area in need of special attention in this pursuit is propulsion. Currently existing propulsion hardware, with the exception of a few new developments[2], will likely not meet the design constraints imposed by microspacecraft. At present, several activities, in various stages of research and development, are underway in the propulsion field to address these issues[2]. Most of this work naturally focuses on thruster hardware. However, improvements in valve technologies with respect to mass, size and power are also crucial to the success of micropropulsion concepts since it is important to ensure that the entire propulsion system weight is reduced.

In this paper a newly proposed, normally closed isolation valve concept will be discussed which is based in its fabrication on MEMS (Microelectromechanical Systems) technologies, resulting in a valve body approximately 1 x 1 x 0.1 $cm^3$ in size and weighing but a few grams, excluding fittings and packaging. MEMS technologies have recently gained increased attention in microspacecraft component designs due to their potential for achieving degrees of miniaturization otherwise unattainable. While more traditional metal-fabricating "machine-shop" technologies have shown impressing reductions in component mass and size[3], MEMS components offer the potentail of a highly integrated, extremely small propulsion system through either chip-to-chip bonding or integration on the same chip of various propulsion components, such as thrusters, filters and valves. Integration may even include the necessary control and power conditioning electronics, in particular in silicon-based systems. The resulting propulsion module would be characterized by its extremely small size and weight, as well as minimal external interfaces, which should simplify integration into the spacecraft and the costs associated with it considerably.

Unfortunately, currently available MEMS valve technology, as provided by the non-aerospace industry, does not appear to meet many requirements of spaceflight application, such as leakage rate requirements, valve actuation times, required voltage bus requirements, or robustness of design. One of these short-comings, namely leakage concerns, may be addressed by the here proposed valve concept. Acting as an isolation valve, it could provide essentially zero-leakage rates prior to actuation of the valve, thus simulating a conventional pyro-valve used in macro-propulsion systems. However, as will be seen below, no pyrotechnic actuation will be required in this valve concept. Using this valve will allow feed systems to stay perfectly sealed until their time of actual use. In the case of certain interplanetary missions, this time interval may range between several months to several years over which considerable leakage could occur using an un-isolated system.

While targeted for microspacecraft use, applications of the micro-isolation valve may also be found in more conventionally sized propulsion systems requiring only low flow rates, compatible with the to be expected small flow dimensions that could be provided on a chip. Such criteria may be

fulfilled by certain electric propulsion systems, such as advanced ion and Hall thruster systems, requiring substantial dry weight reductions in its feed system designs.

In the following sections the micro-isolation valve concept will be introduced, key feasibility issues will be identified, and initial tests and analysis aimed at addressing these issues will be discussed.

## II. DESCRIPTION OF CONCEPT

### Concept

The micro-isolation valve in its current form is a micromachined, silicon based device that relies on the principle of melting a silicon plug, possibly doped to enhance electrical conductance, which in the valve's normally closed position blocks the flow passage. Melting of the plug will be achieved by passing an electric current through it and resistively heating it. The valve will thus serve a similar function as a normally-closed pyrovalve, providing an essentially zero leak rate prior to actuation by completely sealing the flow passage. Unlike a pyrovalve, however, the here proposed valve will not rely on pyrotechnic actuation, thus avoiding the potential for pyroshocks as well as simplifying valve integration.

A schematic of the valve can be seen in Fig. 1. It consists of two basic components: the silicon chip featuring all the flow passages and inlet and outlet, and a Pyrex cover to seal the flow passages while allowing to view the internal of the chip for experimental evaluation of the concept. Later versions may be entirely assembled from silicon. The silicon-Pyrex bond is achieved by means of anodic bonding, a standard bonding technique in microfabrication by which silicon and a special grade of Pyrex (Dow Corning 7740) are placed in immediate contact with each other. Applying pressure and an electrostatic potential across the bond surface at a temperature of approximately 450 C causes the two chips to fuse together. The bonding mechanism is believed to be due to the formation of a thin silicon oxide layer along the bond surface and is thus chemical in nature. Very strong bond strengths can be obtained using this technique as will be seen below.

The silicon side of the chip features the plug, the valve-internal flow channels and a filter, and will be batch-fabricated from larger silicon wafers. Propellant entering the valve chip will flow through a short channel section etched into the silicon side of the chip until it reaches the plug. Channels in the chip are fabricated using deep trench reactive ion etching (RIE) techniques. This etching process is highly directional and allows deep features to be etched into the chip with very

straight wall sections up to aspect ratios as high as 30:1. Metal (gold) leads deposited onto the silicon substrate, partly overlapping the doped-silicon plug region, and connect the plug to an external valve-opening circuitry. Passing an electrical current through the plug will melt and/or vaporize it and propellant located upstream of the valve inlet will push the plug debris downstream, thus opening the valve.

Beyond the plug location the flow path continues. In order to prevent plug debris from contaminating flow components located downstream of the isolation valve, potentially clogging propellant lines, contaminating valve seats or otherwise interfering with the proper function of those components, it is crucial to trap the debris within designated, non-critical regions of the valve without re-closing the flow path again. It is being speculated that due to the melting, rather than cold fracture, of the plug debris count may be reduced and fewer, larger debris particles may be produced, which will be easier to trap. Nonetheless, filtration and other debris trapping schemes will be required.

Figure 1 shows one potential flow path configuration designed to accomplish this task. Here, the flow path goes through a series of S-shaped turns designed to trap molten plug debris in the corners of the etched channel. Oversizing the channel, in particular near the corners, will avoid clogging. Other configurations may be explored as the experimental program progresses, such as parallel flow passages for redundancy, for example. A comb filter integrated in the flow path downstream of the S-shaped condensation region will serve to trap debris that may not have been condensed at the flow path walls, and instead have solidified in the propellant stream. The comb filter uses a staggered filtration scheme , consisting of several rows of silicon posts. The spacing between posts decreases for rows located further downstream, allowing larger particles to be trapped by upstream rows with wider post spacings and smaller particles by rows with narrower post spacings located further downstream, thus avoiding clogging of the filter. Using MEMS-based techniques, it is expected that very small filter ratings may be produced, into the μm-range.

## Key Feasibility Issues

Reviewing the intended operating scheme of the micro-isolation valve, several key feasibility issues can immediately be identified and will need to be addressed in the ensuing research program. Among these issues are:

(1) *Plug Melting*: Melting of the plug will need to be achieved within acceptable energy constraints. Energy storage devices, such as capacitors, may be used to provide suitable power levels over the

valve actuation period. Melting should be achieved quickly to limit heat conduction losses to the remainder of the chip where high temperatures could lead to thermal stresses, in particular between bonded components that feature a coefficient of thermal expansion (CTE) mismatch. In the case of the discussed laboratory devices this mismatch may occur between silicon and Pyrex, in particular above temperatures of about 300 C where the CTE values of Dow Corning 7740 Pyrex and silicon begin to diverge. Even in the case of future, all-silicon versions of this valve mismatches may still occur between the valve and packaging.

(2) *Pressure Handling Capabilities:* The micro-isolation valve chip will be required to maintain large internal pressures in particular in the case of gaseous propellant applications, such as some electric propulsion systems. Typical gas storage pressure in a xenon feed system are around 2000 psia (13.6 MPa). Since factors of safety of 1.5 are typically required, burst pressure may have to be as high as 3000 psia (20.4 MPa). This poses a major design challenge given that the chip consists of silicon and glass. Of particular interest in this context is also the plug. Thermal considerations, alluded to above, will drive the plug dimensions to smaller widths in order to minimize power requirements for melting. Pressure requirements, on the other hand, will drive the plug design into the opposite direction.

(3) *Contamination Related Issues:* Trapping of plug debris inside the micro-isolation valve chip is crucial to the success of this valve concept. No debris can be allowed to propagate downstream into other flow components, in particular not onto valve seats that may be located downstream of the isolation valve. For micropropulsion applications in particular, these valve seats may themselves be very small in size, thus resulting in tight filter rating requirements. In principle, micro-machined comb filters may offer a solution in this regard, and will need to be experimentally verified.

Both items (1) and (2) have been addressed in this paper and show promising results. Given the interrelationship of thermal as well as structural (burst pressure) considerations in the plug design, plug melting and valve burst pressure tests were addressed simultaneously in this study. Contamination and filtration issues will be considered in follow-on testing. In the following sections thermal finite element modeling of valve plug designs will be discussed, allowing initial estimates of power requirements and valve actuation times, as well as burst pressure test results obtained for the several test chips will be reported on.

## III. THERMAL MODELING OF PLUG DESIGNS

In order to determine an appropriate valve plug design, the plug region of the valve was modeled thermally using a finite element package. The Finite Element Analysis (FEA) software used

was PATRAN 6.0. The model of the plug region of the valve contained about 10,000 elements. In order to conserve computation time, only a quarter section of the plug, cut along two lines of symmetry, was modeled. In line with test chip design and fabrication considerations, the plug dimensions were chosen as 300 x 300 $\mu m^2$, and two plug thicknesses, 10 μm and 50 μm, were considered. The thinner plug barrier will represent a thermally favored design, since melting this barrier will be easier to accomplish, while the thicker barrier, as will be seen in Section IV, will be favored based on pressure handling considerations.

Heating of the plug will occur resistively by passing an electric current through it. Since silicon is a semiconductor, it may be required to dope it to increase its electric conductance. Fabrication constraints are such that doping can only be achieved up to certain depths into the silicon due to diffusion limitations. Even using ion implantation with a combined thermal drive-in, doped thicknesses of more than 10 μm can usually not be achieved. In the fabrication of the micro-isolation valve wafers that feature epitaxially grown doped silicon layers are therefore being considered. These layers may be grown up to thicknesses of about 40 μm. Currently we have access to wafers featuring a 25 μm thick doped silicon epi layer. Thus, in the calculations it is assumed that heat is deposited into the barrier only over a thickness of 25 μm, as measured from the top of the barrier. All calculations were performed for a normalized 1W total heater input power. Since this model relies entirely on heat conduction, defining a linear relationship between temperature and power, temperature values can easily be extrapolated to other power levels. Test cases with this model were run to confirm this approach.

Figure 2 shows the case of a 10 μm thick plug (barrier) wall. Represented in this Figure is, as discussed, only a quarter section of the plug area. This section was obtained by both cutting the channel length-wise, along its center line, and, in a perpendicular direction to the previous cut, dicing the barrier along its center plane. The part of the section extending above the height of the barrier wall in Fig. 2, i.e. the upper third of the section, represents the Pyrex cover. The lower two-thirds of the section represent the silicon wafer. The flow channel can be seen extending behind the plug. Thus, as represented in Fig. 2, only half the width and half the thickness of the barrier and only half the width of the channel extending behind the barrier is shown. Propellant would thus either flow into or out of the plane of the paper, if the barrier was open, depending on flow direction.

As can be seen by inspecting Fig. 2, the peak temperature in this 1-W case reaches a value of 232 C in the center of the barrier near its top, where it bonds to the Pyrex, after only 0.3 ms. Thus, for a case of 10 W input power, which even without energy storage devices is not an unreasonable power level for a microspacecraft application , this temperature would be as high as 2320 C. Silicon melts at 1400 C. Thus, for a 10 W case, a substantial fraction of the barrier, approximately representing the upper 20% of the barrier, would reach melting temperatures, as can be seen by following the temperature contours in Fig.2. However, as the barrier starts to heat from the top where the electric current is flowing, the upper 25 μm, upon reaching melting temperature, may be removed, and the plug may thus loose the ability to conduct current and further heat addition may be prevented. Using the temperature plot in Fig. 2 results in a power estimate of about 7 W for a duration of 0.3 ms to melt the barrier to a depth of 25 μm measured from the top. These considerations do of course not take into account any influence the propellant pressure may exert onto the barrier. It is conceivable that due to softening of the silicon barrier prior to melting, and the application of pressure onto barrier, even regions of the barrier which are below the actual melting point may break and be opened up.

Figure 3 shows the case of a plug of 50 μm thickness. Calculations were again performed in the normalized case of 1 W power consumption. After an on-time of 0.5 ms, comparable to the previously discussed 10-μm plug case, peak temperatures reached a value of about 58 C. Thus, in order to reach at least 1400 C in a comparable time period, approximately 1400/58.6 * 1 W = 24 W of power would be required over a duration of 0.5 ms. Given that the peak temperature shown in Fig. 3 is only reached at one location just below the top of the barrier, slightly higher power levels will likely be required in practice to heat the barrier to melting temperature to a depth of 25 - 40 μm, depending on doping thickness. Using the plot in Fig. 3, for a melting temperature of 1400 C to a depth of 25 μm one may estimate a power requirement of about 28 W over a duration of 0.5 ms.

While it may not be possible to remove the barrier in its entirety, an orifice located at the upper end of the barrier of about 25 - 40 μm in depth and of a comparable or larger width appears sufficient to allow for sufficient flow rates at very little pressure drops, even for liquid propellants, as was found out in related micropropulsion experiments recently conducted and discussed in a companion paper[4]. In that experiment, a vaporizing liquid micro-thruster chip featuring a 50 x 50 $\mu m^2$ inlet and a 50 x 50 $\mu m^2$ outlet, separated by a channel of similar dimensions and length as the one considered for the micro-isolation valve, showed no problems in passing appreciable amounts of fluids (water) at

feed pressures of 10 psig and less. The flow channel dimensions in the micro-isolation valve will continue to be kept larger than the expected orifice in the barrier to reduce pressure drops inside the chip and to help avoid clogging of flow passages, in particular downstream of the plug region.

Thus the thermal analysis performed here seems to indicate that valve actuation is possible within power/energy levels that may still be available on a microspacecraft, although these values are somewhat on the high side, in particular for the thicker plugs. For applications in larger systems, such as future electric propulsion feed systems, where ample power should be available, this may not be a concern. The aforementioned numerical results obviously need to be verified through experiments. Such experiments are scheduled immediately after completion of burst pressure tests to be discussed next.

## IV. BURST PRESSURE TESTS

### Test Chip Design

As was mentioned in Section II, valve plug design will be governed by two predominant, yet conflicting, requirements. Thermal considerations, as discussed above, will favor a thin plug design to reduce power requirements to melt the barrier. Requirements with respect to pressure handling capability, on the other hand, will drive the design to larger plug thicknesses. In order to finalize the plug design, a series of tests was thus conducted to determine burst pressures for different plug thicknesses and valve body configurations. An experimental, rather than a numerical, approach was chosen to evaluate pressure handling capabilities of valve chips due to the expected statistical variation inherent in such tests, possibly depending on small material defects, which would have exceeded modeling capabilities. Strengths of the anodic bonds between the silicon and Pyrex along the top of the barrier would also have been difficult to model accurately, but may influence the results considerably.

In order to perform these tests, a series of dedicated test chips was fabricated. One of these chips is shown in Fig. 4 and a schematic outlining some of its design features is depicted in Fig. 5. This chip design will be referred to as "Batch-1" in the remainder of this paper. The chip design focuses solely on the plug region and the optimization of the plug design, and thus does not yet contain any measures to trap plug debris. Besides being used for burst pressure tests in this test run, it will also be used in plug vaporization tests. The chip features a straight, 4 mm long channel section with a cross section of 300 x 300 $\mu m^2$. The plug is located in the center of the chip, dividing the

channel section in two halves. Several different plug designs were tested, ranging in thicknesses from 10 μm to 100 μm. The channel is connected to an inlet and outlet through which gas can enter and exit the chip from the silicon surface. The chip is sealed with an anodically bonded Pyrex cover. This seal necessitates the fabrication of two recesses into the chip which feature the electric leads to the plug, visible as the lightly-colored rectangular regions in Fig. 4. Since metal deposition may be as thick as several tenths of a micron, depositing the metal lead directly onto the non-recessed silicon surface would have led to leakage paths immediately adjacent to the metal deposits, as the Pyrex would have been forced to bent over them.

Although doping of the silicon is possible to provide electric contacts, its resistivity is higher than that of gold, and since the desire was to create the majority of the voltage drop in the plug region were heating was supposed to occur, gold was chosen as connecting material. The chip itself can then be electrically contacted near the edges, were notches in the Pyrex (see Fig. 4) are provided for this purpose. Contacting the chip near its edges is preferred as it minimizes the wire length needed for wire bonding. These wires are typically very thin and fragile and minimizing their lengths simplifies handling of the chip.

No current input was needed for the burst tests. However, since the recess may impact the pressure handling capability of the chip, it was integrated into the chips used for burst testing. The reason for this may be seen in Fig. 5 and also in Fig.6. Due to the recess, there exist regions of minimal bond width between the pressurized channel and the recess for the metal leads. Across these regions debonding and leakage may occur at very high internal pressures. As will be seen below, this did indeed occur at pressures exceeding 1800 psig (12.2 MPa). For this reason a second chip design was also tested.

This second batch of chips, referred to from here on as "Batch-2", is shown in a schematic in Fig. 7. This design features narrowed recess regions (only 1.5 mm in width) for the metal leads. This increased the overall silicon/Pyrex bond area. Another new design feature was added to this chip. Wrapping around the recess area and the entire channel section is a narrow 25 μm wide isolation trench, as can also be seen in Fig. 8. This trench serves as an electrical insulation: As was pointed out in Section III, in order to create a large enough opening in the barrier, the silicon surface may have to be doped to a sufficient depth. More conventional doping techniques such as ion implantation, followed by a thermal drive-in, could only provide sufficient doping to a depth of about 10 μm. However, the advantage of this technique is that it can be tailored to certain regions of the chip only.

Using doped epi-wafers, doped silicon regions as thick as 40 μm may be grown on a silicon substrate wafer. In this case, however, the entire chip surface is doped, and not only the plug region. This could allow current to flow around the channel section to the opposite metal lead, potentially shorting the plug. To create a high resistivity path for the current around the channel section, the trench narrows the region along which current may flow to 200 μm, which is the separation between the isolation trench and the channel. (Obviously the trench may not intersect with the channel as a leakage path would be created through the trench). Again, for burst testing, since no current flow was intended, this design feature would not have been needed. However, since it may impact pressure handling capability as it locally decreases bond widths, this design feature was included in the burst tests.

## Chip Fabrication

The fabrication of the micro-isolation valve is a combination of silicon etching and wafer bonding techniques. Desired features are first etched in silicon to create the device's structure and then the chip is pressure sealed by anodically bonding a Pyrex wafer to the silicon. Etching of silicon is achieved using a Deep Trench Reactive Ion Etching (RIE) system available at JPL's Micro Devices Laboratory (MDL). This Deep Trench RIE system, which is manufactured by Surface Technology Systems, Inc. (STS), provides highly anisotropic etching parameters in silicon. The fabrication of these structures results from the utilization of an alternating inductively coupled plasma of $SF_6$ and $C_4F_8$ gases[5]. Etching of exposed silicon areas occurs during the $SF_6$ plasma step where a fluorine-rich environment chemically reacts with and removes silicon from the wafer. The $C_4F_8$ step in the etching process is used to control the anisotropy of the etching by passivating the sidewalls of the etched features. This steps helps to prevent lateral etching (i.e. undercutting) of the silicon features as well as the mask layer during the next etch step. The STS system can provide silicon etching rates of about 4.5 μm/min, aspect ratios of 30:1 and sidewall angles of $90\pm<0.25°$. Figure 8 shows the results obtained with this etching technique. Note the straight channel walls and the thin, vertical barrier (i.e. "the plug") intersecting the channel.

## Burst Test Set-up and Procedure

The burst test set-up is shown in Fig. 9. The chip was bonded to a stainless steel fixture, connecting the inlet and outlet holes of the chip to two tube stubs featuring Swagelok® fittings. One fitting was connected to the pressurant supply while the other was connected to a leak detector, thus allowing for valve internal leak checks across the plug. External leaks were monitored by determining

the pressure decay in the system, i.e. if no internal leak could be registered with the leak detector, yet pressure decayed, the leak was determined to be external. The entire chip assembly is placed into a test barricade for protection during burst tests. The pressurant supply provides regulated helium pressure to the valve inlet. Pressure is measured with a 0-5000 psig pressure gage, mounted directly upstream of the chip, to an accuracy of $\pm$ 0.25%. The test procedure begins with a slow purge and vent of the entire upstream pressurant system (up to the valve chip plug) to fill the system with helium. The pressure is then slowly increased in 100 psig steps and held at those increment levels to check for external (through pressure decay) and internal leaks across the chip barrier (with the leak detector).

**Results - "Batch-1" Type Chips**

Results obtained for Batch-1 type chips are summarized in Table 1. This table lists a chip identification number, the burst pressure or the pressure at which leakage (external or internal) occurred, the mode of failure (external leak, internal leak or burst), the plug width and the bond widths to both sides of the channel, formed by the boundaries of the channel and recess, respectively (compare with Fig. 6). Although intended to be equal, a slight misalignment of masks caused the bond width to one side of the channel to be bigger than the one on the opposite side. All the chip dimensions were measured under an electron microscope. This was possible, as will be seen below, because the Pyrex cover glass blew off the silicon side of the chip at the time of failure. In the cases were this did not occur (Chips # 2 and # 6), this was not possible since Pyrex is not transparent when observed under an electron microscope. Thus the nominal plug widths were listed in Table 1 for these chips instead, and sidewall bond widths could not be listed.

As can be seen, chips featuring 10 μm wide plugs suffered from internal leakage. Inspection of the chips after the test showed that the bond between the top of the barrier and the Pyrex had failed. It had been noted by the authors before that good anodic bonds to very thin structures were difficult to achieve and one of the goals of this test was to study the integrity of these thin bonds. Chips with somewhat larger bond widths (27 and 38.8 μm) performed better, however, burst failure of the chip occurred at comparatively low pressures of 1050 psig (7.4 MPa ) and 900 psig ( 6.1 MPa). In the case of Chip #13, failing at 900 psig (6.1 MPa), the bond widths next to the channel were rather small when compared to the other chips, with a minimum bond width of only 22.5 μm, and may thus explain the lower burst pressure. Chips with even thicker plug widths (59 μm and 100 μm ) and

larger bond widths along the channel walls performed better, reaching burst pressures as high as 1850 psig (12.6 MPa).

The burst failure mechanism for these chips was always the same and results obtained from these tests can be seen in Fig. 10. The particular chip shown in this Figure is Chip #12. As can be seen, that portion of the Pyrex covering the inlet side of the chip was blown off. It thus was clear that the anodic bond between the silicon and Pyrex had failed. Consequently, a redesign of the chip was pursued, leading to the "Batch-2" design described above, featuring larger bond widths. Results are described below.

**Results - "Batch-2" Type Chips**

A total of 30 "Batch-2" type chips was tested in three different test series. Unfortunately, almost all chips of Test Series #1 and #2, with the exception of one chip each per test series featuring a 50 μm plug, failed at very low pressures, not exceeding a few hundred psig. Upon post inspection, it was noted that the plug barriers had thinned during fabrication towards the bottom of the channel, and that the barriers had broken predominantly at these locations. Since the exact plug thickness could not be determined at these locations due to visual inaccessibility, all tests of Test Series #1 and #2 were dismissed, with the exception of the two tests performed with the 50 μm plug chips. Since in these cases the plugs did not fail, and, as will be seen below, the failure mode at burst was not related to the plugs, data obtained with these chips could be used.

Chips in Test Series #3 all featured a very homogenous plug thicknesses, and 15 chips were burst tested in this series. Data obtained with these chips and the two remaining chips from Test Series #1 and #2 are listed in Table 2. A clear trend towards higher burst pressure with increasing plug thickness can be noted. Plug thicknesses of 10 μm can maintain a few hundred psig pressure before the plug barrier breaks, 15 μm plugs can maintain up to about 1000 psig, and 20 μm plugs can sustain up to about 2,300 - 2,600 psig. Plug barrier failure usually appears as shown in Fig. 11. It is interesting to note that, while the barrier breaks away, fragments of the barrier remain attached to the Pyrex cover, indicating the strength of the anodic bond.

However, beginning with 20-μm chips, and exclusively for the 25, 35, and 50-μm chips, the failure mode changes. For these chips, at burst pressures ranging as high as 2,650 - 2,900 psig, the plugs remained intact, however, a piece of Pyrex typically located directly above the inlet hole was

blown out as can be seen in Fig. 12. Note that the Pyrex did not detach from the silicon substrate, as was observed for "Batch-1" type chips. Thus, Pyrex failure, rather than anodic bond failure, was believed to be the cause for the burst of this type of chips, whereas the plugs are able to withstand these pressure levels.

It should also be noted that some of the valves (namely #4 and #5 in Table 2) failed at very low pressures, in the case of valve #4 this may have been due to the small plug width, in the case of #5 a leak across the top of the plug barrier, where bonding is supposed to occur between the silicon material of the plug and the Pyrex cover, may have occurred.

Several conclusions may be drawn from these tests:

(1) Burst pressures obtained with isolation valve chips, in particular those featuring 50 μm wide plugs, are highly impressive, considering that the valve chip is fabricated entirely from silicon and glass.

(2) The increased bond area between the Pyrex and silicon substrate in the "Batch-2" type chips versus the "Batch-1" type chips appears to have served its purpose of increasing overall bond strengths, since Pyrex no longer debonds in the "Batch-2" cases.

(3) It seems possible that burst pressure values for "Batch-2" type chips featuring plugs of at least 25 μm thickness could easily be extended to even higher values through the use of thicker Pyrex. Figure 13 displays obtained burst pressure values versus plug widths. Clearly, the two failure modes (plug failure for plugs $\leq 20$ μm, Pyrex failure for $\geq 20$ μm plugs) can be distinguished by the abrupt bend in the solid curve, carried on as a dashed line to the data points obtained for the 25, 35 and 50 μm plugs. Had the Pyrex not failed, an extrapolation of the solid curve would point to clearly higher burst pressure values for the 25 μm and larger plugs. Given the scatter of the data, however, it is not recommended that a quantitative burst pressure value for plug widths > 20 μm value be deduced from such an extrapolation. Current Pyrex thickness is 0.5 mm. Thicker Pyrex, possibly up to 1 - 1.5 mm thickness may be tested to verify this assumption. Pyrex wafer thcker than 1.5 - 2 mm may not be successfully bonded anymore using currently available anodic bonding equipment. Beyond the current test program, which will require optical access to the valve interior for test evaluations, non-transparent, all-silicon chips may be explored, where Pyrex would be replaced with stronger silicon

material. Note the positive slope of the dashed curve indicating the Pyrex failure mode. This slope should not be expected if Pyrex failure is the cause. It is unclear at this point whether this is a consequence due to the scatter of the limited amount of data, or a real physical effect. It was noted for the chips #12 and #C5*, i.e. those chips featuring the lowest burst pressure values for any of the Pyrex failure mode cases, that a larger portion of the Pyrex located over the inlet side of the chip had been torn out, possibly pointing to a weakness in the Pyrex or a poorer anodic bond for these particular chips. Chips with identical plug sizes are typically located within close proximity to each other on the wafer during fabrication. If a material defect was located in the Pyrex material or bonding was not perfect at this location during fabrication, it could explain the proneness to failure for these 20 μm plug chips.

(4) Depending on the application, plug sizes could be tailored to the actual pressure needs. A liquid propellant application, for example, typically featuring much lower feed pressures of only 300 psia or so, may only require a 15 - 20 μm thick plug, which would reduce power requirements to melt the plug. Cold gas applications will require larger plug thicknesses depending on storage pressure. Ten micron plugs appear not very useful for typical propulsion applications given here obtained set of data.

## V. PRELIMINARY SYSTEM DESIGN IMPLICATIONS

Examining numerical plug melting investigations and burst test results, it appears that plug thicknesses of at least 15-20 μm and power levels to actuate the valve of 10-30 W will be required even for low pressure liquid applications. This will have important ramifications for the overall system design, in particular its power conditioning circuitry. Power levels that high may be at the maximum limit available on microspacecraft. Therefore, the micro-isolation valve may require a dedicated power storage system, such as a capacitor, which may temporarily boost power available for valve actuation. In order to keep the overall system comparable in weight and size to the valve itself, MEMS-based capacitor designs should be explored. While at first sight it appears relatively trivial to manufacture such a capacitor (two thin-film conductive, e.g. metal, layers separated by an insulating, e.g. silicon dioxide, layer deposited on a silicon substrate for rigidity), available surface areas in such a device would be small, limiting achievable capacity values. For example, assuming a total surface area of 10 $cm^2$ (corresponding to ten stacked 1 $cm^2$ capacitors, each about the size of the valve, packaged into a volume of. approximately 1 $cm^3$), the achievable capacity can be calculated according to

$$C = \varepsilon_0 \ \varepsilon \ \frac{A}{d} \qquad (1)$$

with $\varepsilon_0 = 8.859 \times 10^{-12}$ $A^2s^2/J$ m and $\varepsilon = 3.9$ for silicon dioxide filling the gap between the capacitor plates, d being the gap between the capacitor plates assumed at 2.0 μm in this example, and A the area assumed as above, as

$$C = 17 \ nF$$

Assuming conservatively, despite observations made in context with Fig. 13, that a 50 μm plug will be required, demanding a power level of 30 W for a duration of 0.5 ms according to the finite element calculations of Section III, and further assuming for simplicity that the total energy required to open the valve can simply be obtained by the product of this power value and the corresponding time interval, the required energy to melt the plug is

$$E_V = 0.015 \ J$$

While this may seem like a very small value, given the small capacitance one can calculate a required capacitor voltage according to

$$E_V = \frac{1}{2} \ C \ U_0^{\ 2} \qquad (2)$$

as

$$U_0 = 1328 \ V$$

According to Ref. 6, using a breakdown field strength of approximately 700 V/μm this voltage value is only slightly less than the breakdown voltage of LTO (Low Temperature Oxide) silicon dioxide for a gap of 2 μm. This voltage requirement is very high and would require dedicated voltage transforming capabilities. Again, in order to maintain the mass and weight advantage of the isolation valve concept, this transformator itself may have to be micromachined, possibly be MEMS-based in order to allow for easy integration with the valve.

An alternative approach might be to search for ways to increase capacitances achievable with microfabricated capacitors. In principle, one may conceive of a device consisting of multiple alternating layers of silicon oxide (representing the insulator) and a suitable thin-film metal (representing the capacitor plates) to be deposited on a substrate. Parallel switching of the created capacitors would increase the capacitance available per chip. Since each layer would only have to be a fraction of a micron thick (possibly larger for the insulator to avoid electric breakdown), large capacitances could be built up even on a relatively small chip. In practice, however, there exists a limit with respect to the number of thin film layers that can be deposited onto a chip. Intrinsic stresses present in thin films will eventually built up to the point were films are no longer able to stick to the underlying layers and begin to peel off.

Even if larger capacitances could be manufactured successfully, a second constraint will need to be observed. The time required to achieve a certain depth of discharge for a capacitor is proportional to the product of ohmic resistance in the circuit and its capacitance, i.e. RC. Since the micro-isolation valve requires a fairly rapid deposition of energy into the plug to avoid thermal diffusion losses to the remainder of the chip where thermally induced stresses could lead to delaminations between the chip package and the chip, or the Pyrex and silicon layers within the chip, a larger capacitor may no longer be fully discharged within this time limit. This will require the capacitor to be charged to higher energy levels than are required for melting of the plug. Thus, although the larger capacitance will drive voltage requirements for the capacitor down, the higher initial stored energy requirement will counteract this trend to some extend. The following analysis will clarify this issue.

The energy stored within the capacitor connected to a circuit of ohmic resistance R after a time interval t is according to

$$E(t) = \frac{1}{2} C U(t)^2 \quad (3)$$

with

$$U(t) = U_0 \exp(-t/RC) \quad (4)$$

equal to

$$E(t) = \frac{1}{2} C U_0^2 \exp(-t/2RC) \quad (5)$$

Thus, the energy transferred to the circuit (i.e. the valve) after time t is then

$$\Delta E = \frac{1}{2} C U_0^2 (1 - \exp(-t/2RC)) \quad (6)$$

where the necessary requirement for valve actuation is

$$\Delta E = E_V$$

Defining

$$\delta = 1 - \exp(-t/2RC) \quad (7)$$

equation (6) can be written as

$$E_V = \frac{1}{2} C U_0^2 \delta \quad (8)$$

where $\delta$ is the fraction, in terms of stored energy, to which the capacitor is being discharged.

Assuming a value for $\delta$, the capacitance can be calculated according to Eqn. (7) assuming a value of R = 50 $\Omega$, the lowest resistance value measured for a micro-isolation valve to date, and t = 0.5 ms in accordance with thermal FEA calculations of Section II. Using the calculated value for the capacitance, as well as $E_V$ = 0.015 J and $\delta$ again yields the required initial capacitor voltage $U_0$ according to Eqn. (8). The results for $\delta$ and $U_0$ are shown in Figs. 14 and 15.

Figure 14 shows that, as alluded to above, larger capacitances can only discharge smaller fractions of their initial stored energy within the given time constraints since they discharge more slowly. However, since the same energy $E_V$ still needs to be provided to the valve, these capacitors have to be charged to a higher value of initially stored energy. The result is that, while voltage

requirements drop due to the larger capacitance, this drop is limited as a result of the required increased initial charge as can be seen in Fig. 15. According to Fig. 15, even for very large capacitances, voltages of less than about 80 V cannot be achieved if the discharge of $E_V$ = 0.015 J is to be provided to the valve within the 0.5 ms time limit.

Although the drop in voltage compared to the previously calculated value is significant, there is a price to be paid for this improvement. Taking as an example the case of $\delta = 0.5$, one calculates from Eqn (7) a value for the capacitance of

$$C = 7\ \mu F$$

The initial capacitor voltage in this case is

$$U_0 = 92.6\ V$$

However, the required capacitor surface area for a 7 μF capacitor using a capacitor plate gap of 0.2 μm (again in accordance with electric breakdown field strengths values of approximately 700 V/μm extrapolated from Ref. 6) is 405 $cm^2$ according to Eqn. (1). Obtaining these types of capacitor surface areas, even using multiple layers of thin conductive and insulating films on a single chip, and in turn using a multitude of such chips, while, at the same time, trying to maintain a small overall capacitor unit volume may represent a formidable task.

Thus, a new, system level feasibility issue may have been identified for the micro-isolation valve, at least for power-limited microspacecraft applications, either requiring the development of high voltage transformers able to step up voltages to 1 kV or more from microspacecraft bus voltages of 5 V or less, or necessitating the development of high storage chip-sized capacitors in addition to requiring reduced voltage transforming capability. Close examination of the respective technological challenges and potentially achievable goals in developing either one of these components will be required. It should be noted, however, that for application on larger scale systems, such as in advanced electric propulsion feed systems, these issue may play a significantly lesser role, since these spacecraft will provide ample power to satisfy the valve needs.

## VI. CONCLUSIONS AND FUTURE WORK

Development of a newly proposed, microfabricated, normally-closed isolation valve design was initiated. This valve relies on the melting of a potentially doped silicon plug to open an otherwise sealed flow passage. Applications for this device may be found in micropropulsion feed systems, such as those envisioned for microspacecraft in the 10 - 20 kg class and below, or for larger propulsion feed system where only low flow rates may have to be maintained, as in some electric propulsion systems (ion and Hall thruster). The micro-isolation valve would play the role of a normally-closed pyrovalve in conventional systems, however, does not rely on pyrotechnic actuation.

Several key feasibility issues need to be addressed in the valve development, such as the ability to melt a silicon plug at power levels acceptable in a microspacecraft environment, the ability to maintain high valve internal pressures to be of use for a variety of propulsion systems, and the ability to trap plug debris inside the chip through adequate filtration schemes. In the current study, both plug melting as well as pressure handling abilities of the valve were addressed. Both investigations are inter-related with respect to the plug design. Thermal considerations alone would lead to thinner plug widths, since these plugs will be easier to melt, whereas pressure handling considerations will drive the design to thicker plugs. Both issues were therefore addressed simultaneously. Filtration related investigations will follow as this program progresses.

Thermal finite element modeling indicates that plugs of thicknesses between 10 - 50 μm can be melted at power levels ranging between approximately 10 - 30 Watt if applied over a duration of approximately 0.5 ms. Significantly larger time intervals could lead to thermal diffusion of the deposited energy across the chip and lead to delaminations between chip and carrier or various components of the chip due to induced thermal stresses. Since power levels have to be applied over very short time durations, energy storage devices, such as capacitors, dedicated to the valve opening sequence maybe required for microspacecraft use. For use in larger systems, such as in advanced electric propulsion feed systems, where ample power may be available, such energy storage components may not required.

Burst pressure tests of several valve test chips were performed to determine pressure handling capabilities. Dedicated test chips were designed aimed at specifically investigating the critical plug region of the valve. Different plug widths and chip designs were investigated. Building on earlier tests, the final design reached burst pressure values as high as 2,850 psig. Pyrex breakage was determined as the failure mechanism for 50-μm plugs. Pyrex-to-silicon anodic bonds, however, were able to withstand even these high pressures. Given the fact that the entire valve is fabricated from silicon and Pyrex glass, these obtained high burst pressure values are quite remarkable. It is felt that

using a thicker Pyrex, or, in later experiments not requiring visual access to the chip, silicon material, even higher burst pressure may be attained. Thinner plugs break at lower pressure levels. Ten micron thick plugs maintain a few hundred psig, whereas 15 μm plugs maintained up to 1000 psig pressures. Twenty micron plugs were able to sustain up to 2,600 psig. Thus, plug thicknesses maybe tailored depending upon the applications. In lower pressure liquid feed systems, for example, thinner plugs maybe used which will require less power to melt, whereas higher pressure cold gas applications will require thicker plugs.

A possible new system level feasibility issue, involving power conditioning components, may have been identified. Using power requirements of 30 W for 0.5 ms for the valve, chip-sized capacitor banks may have to be charged to very high voltages to store the required energy to melt the valve. Voltage values may exceed 1 kV. Larger capacitances will drive voltage requirements down, however, not below 80 V using the assumption of a 50 Ω valve resistance and maintaining the requirement that the energy to melt the valve plug will have to be discharged within 0.5 ms to avoid thermal diffusion and resulting thermal stresses. This is due to the fact that while larger capacitances allow for lower initial voltages to store the required energy, the required fast discharge times will only allow for a fraction of the stored energy to be extracted from a larger, and thus slower discharging, capacitor. In order to still provide the required energy level for plug melting, the larger capacitor will thus have to be charged to a higher initial energy level, driving voltage values back up to some extend. The consequence of these observations is that either transformer technology able to provide very high voltages (1 kV), or high storage chip-sized capacitors, combined with lower voltage transformers, may need to be developed for microspacecraft use of this valve. These concerns, however, are much less significant in larger spacecraft applications, such as in advanced feed systems for various electric propulsion applications, were ample power can be provided to the valve by the spacecraft.

Future work will focus on these issues, as well as plug melting experiments to verify thermal calculations performed in this study. Finally, with a selected optimal plug design, filtration tests will be conducted.

## VI. ACKNOWLEDGMENTS

The authors would like to thank Mr. Larry Rupel for performing the burst pressure tests, Mrs. Sandee Chavez and Mr. John Rice for performing the packaging of the test chips, and Mr. Jim Kulleck and Mr. Ken Evans for performing many of the SEM scans. The authors would also like to

thank Ms. Lilac Muller and Dr. Thomas George for contributing many ideas in the early design phase of this valve concept.

The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. The work was funded by the JPL Director's Research Discretionary Fund and support is gratefully acknowledged.

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Table 1: Burst/Leak test Data for "Batch-1" Type Chips

| Chip I.D. | Plug Width (μm) | Burst Pressure (psig) | Burst/Leak Mode | Sidewall Bond Widths (μm) |
|---|---|---|---|---|
| 2 | 10 (nominal) | 250 | Internal Leak | N/A |
| 6 | 10 (nominal) | 100 | Internal Leak | N/A |
| 1 | 27.1 | 1050 | Pyrex Debond | 111/68.8 |
| 13 | 38.8 | 900 | Pyrex Debond | 22.5/68.3 |
| 3 | 58.9 | 1650 | Pyrex Debond | 78/124 |
| 8 | 100 | 1750 | Pyrex Debond | 122/64.1 |
| 12 | 104 | 1850 | Pyrex Debond | 68.8/137 |

Table 2: Burst Test Data for "Batch-2" Type Chips

| Chip I.D. | Plug Width (μm) | Burst Pressure (psig) | Burst/Leak Mode | Test Series |
|---|---|---|---|---|
| 4 | 10 | < 150 | Plug Failure | #3 |
| 6 | 10 | 325 | Plug Failure | #3 |
| 9 | 10 | 500 | Plug Failure | #3 |
| C 2 | 15 | 875 | Plug Failure, Small Internal Leak | #3 |
| C 4 | 15 | 1225 | Plug failure | #3 |
| 5 | 20 | < 150 | Internal Leak, Plug Intact | #3 |
| C 3 | 20 | 2575 | Plug Failure | #3 |
| C 5 | 20 | 2300 | Plug Failure and Pyrex Failure | #3 |
| 12 | 25 | 1950 | Pyrex Failure, Plug Intact | #3 |
| C5* | 25 | 1970 | Pyrex Failure, Plug Intact | #3 |
| 2* | 35 | 2230 | Pyrex failure, Plug Intact | #3 |
| 3 | 35 | 2610 | Pyrex Failure, Plug Intact | #3 |
| 2 | 50 | 2650 | Pyrex Failure, Plug Intact | #3 |
| C 1 | 50 | 2725 | Pyrex Failure, Plug Intact | #3 |
| 10 | 50 | 2825 | Pyrex Failure, Plug Intact | #2 |
| C 4* | 50 | 2850 | Pyrex Failure, Plug Intact | #1 |
| C4** | 50 | 2900 | Pyrex Failure, Plug Intact | #3 |

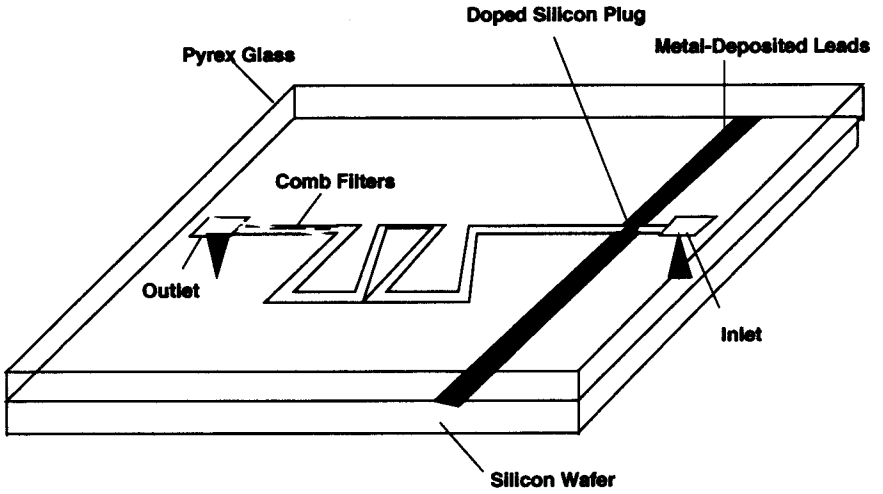


Fig. 1: Schematic of the Micro-Isolation Valve Concept

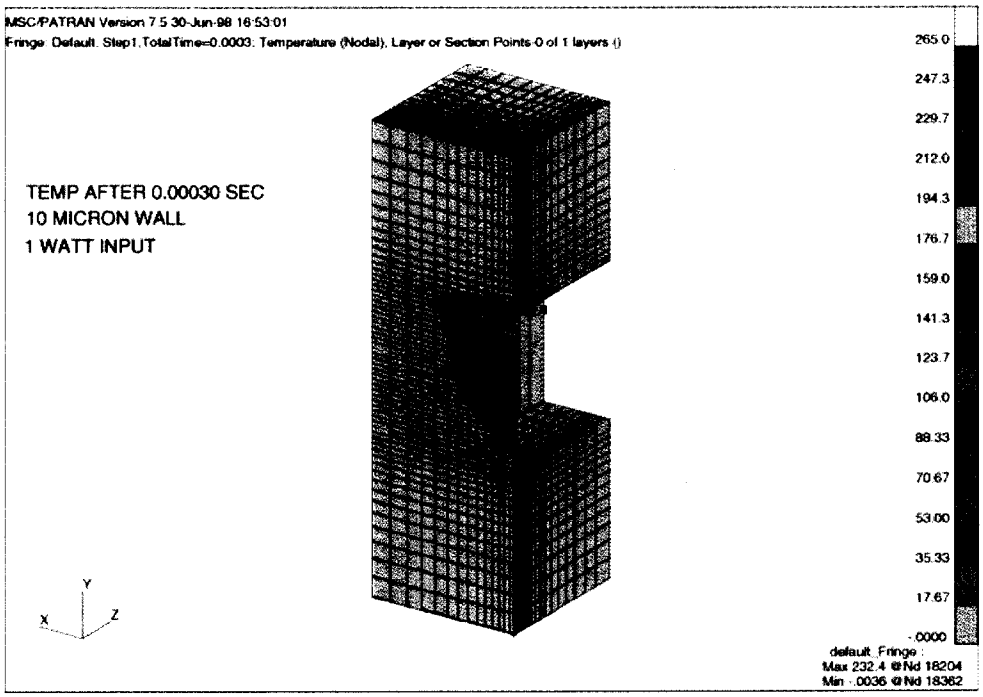


Fig. 2: Results of Thermal Modeling of Plug Quarter Section for a 10 μm Plug Thickness

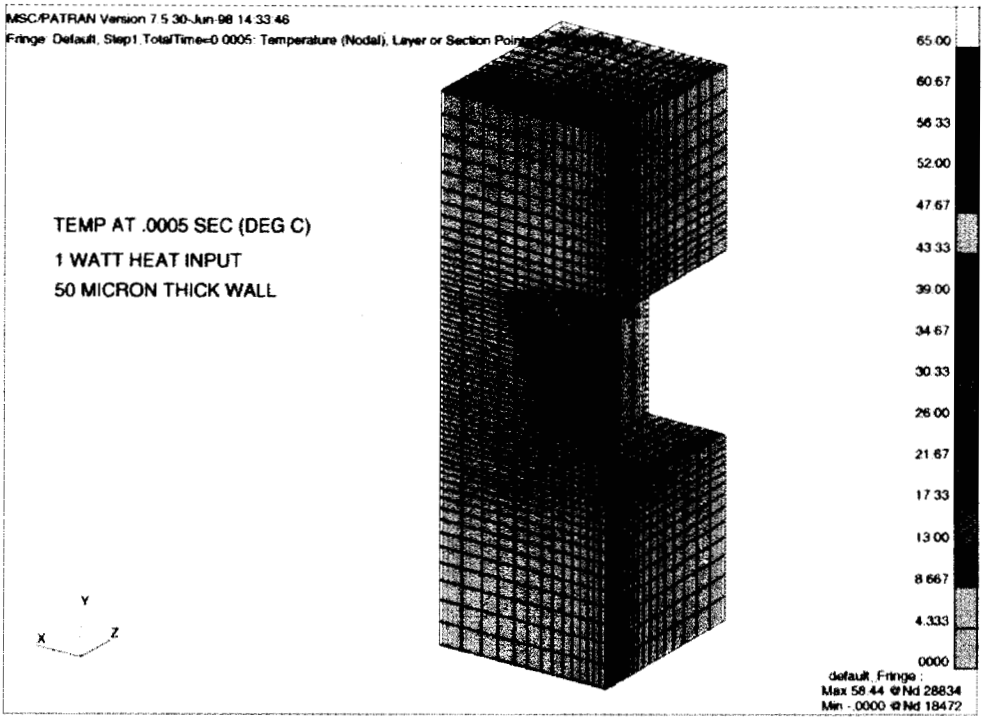


Fig.3: Results of Thermal Modeling of a Plug Quarter Section for a 50 μm Plug Thickness

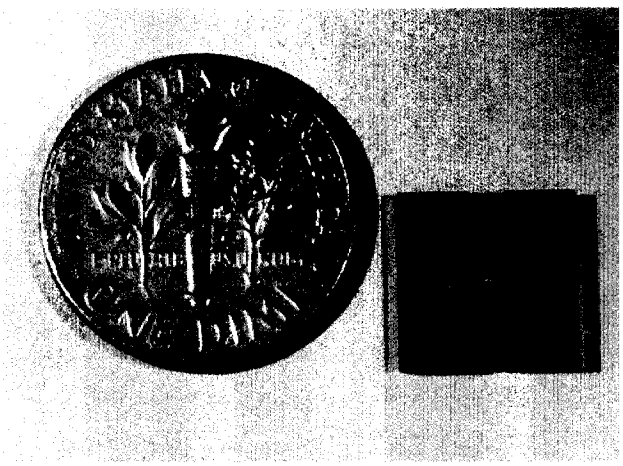

Fig. 4: Micro-Isolation Valve Test Chip

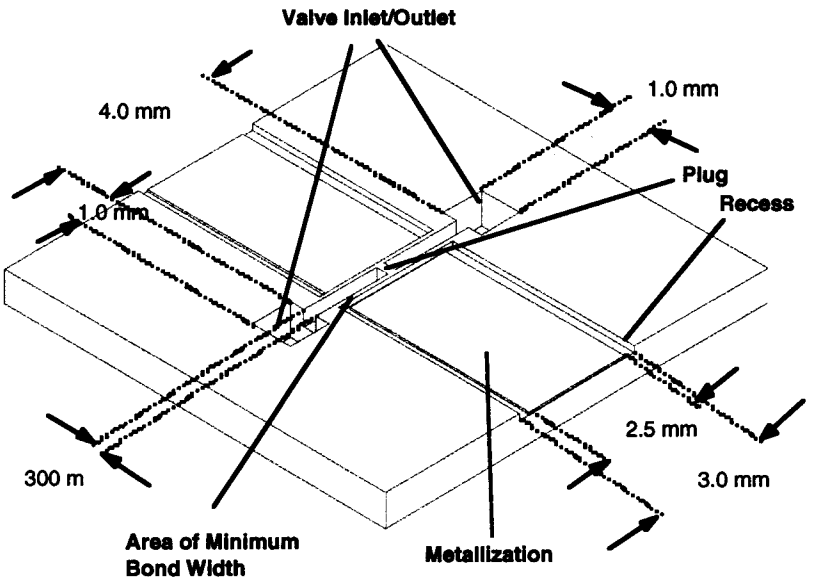


Fig. 5: Schematic of "Batch-1" Type Test Chip

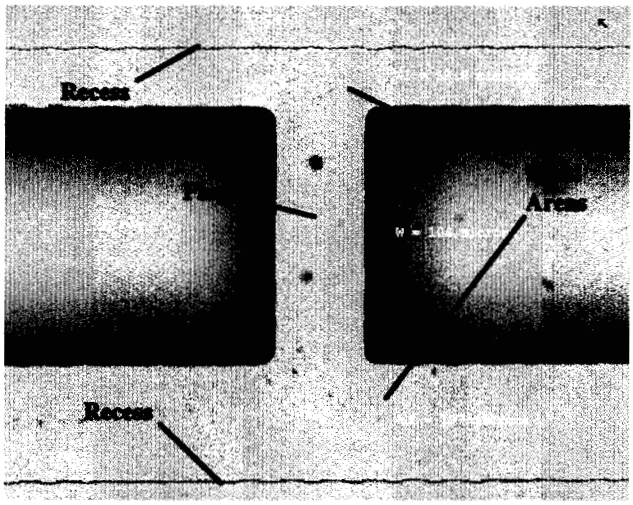


Fig. 6: Close-Up of Plug ("Batch-1" Chip#12)

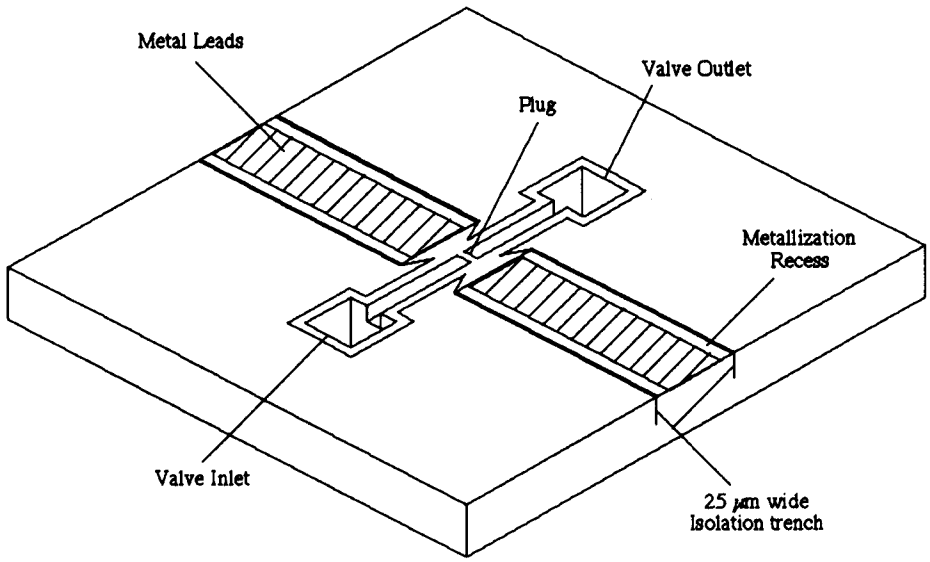


Fig. 7: Sketch of "Batch-2" Type Test Chip

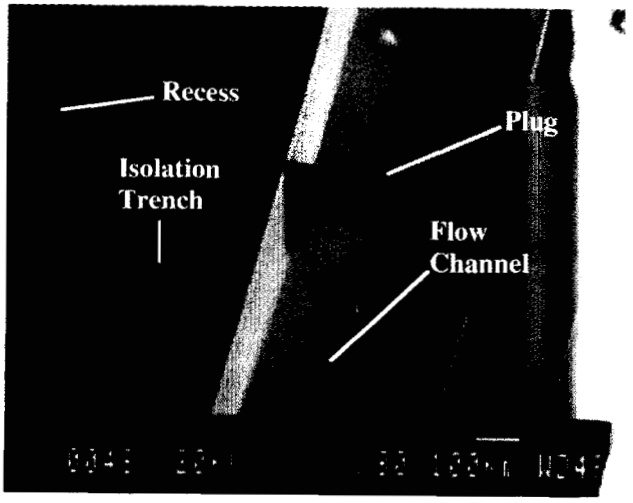


Fig. 8: Close-Up of Plug Area ("Batch-2"-chip) with Recess and Isolation Trench

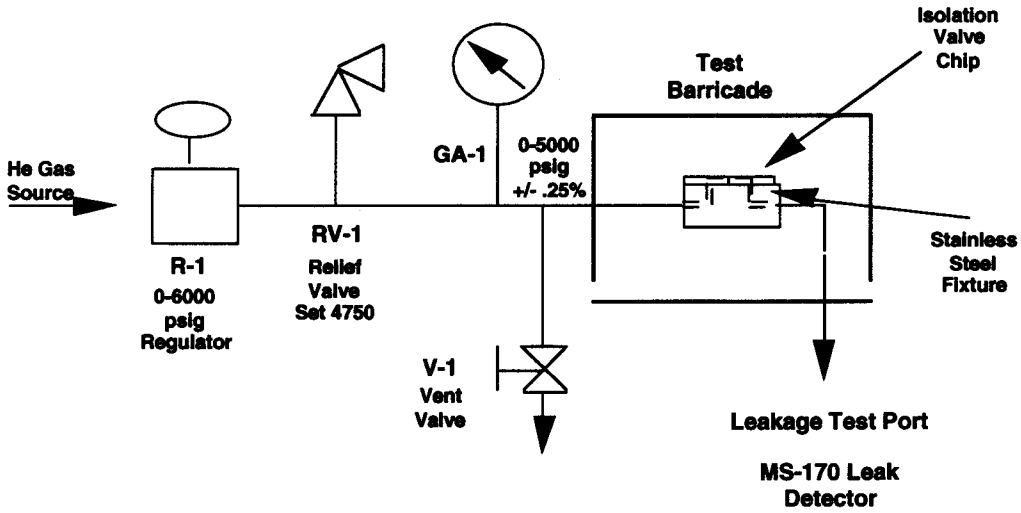


Fig. 9: Burst/Leak Test Set-up

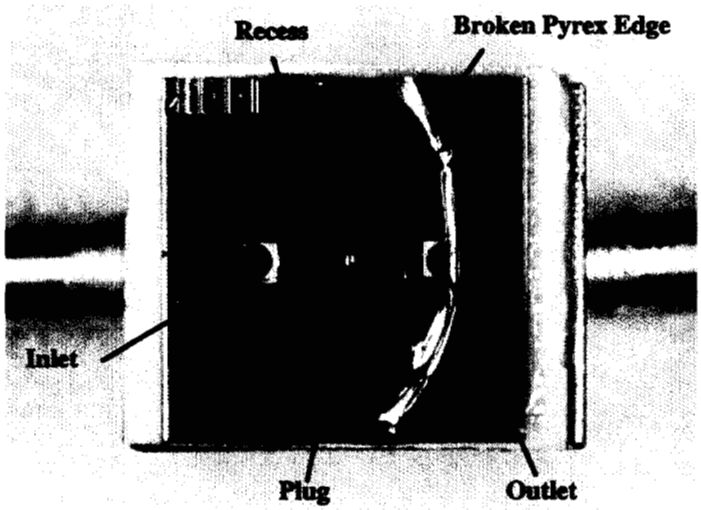


Fig. 10: Post-Test Image of Burst "Batch-1" Type Chip. Notice Pyrex Blown Off.

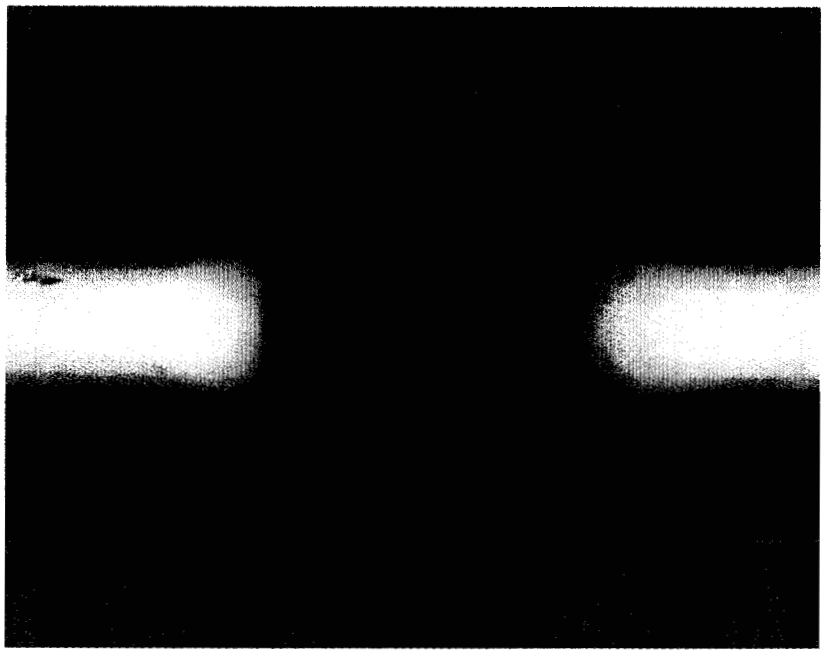

Figure 11: Plug (Barrier) Failure for Chip # C3 (20 μm plug width, Burst @ 2575 psig)

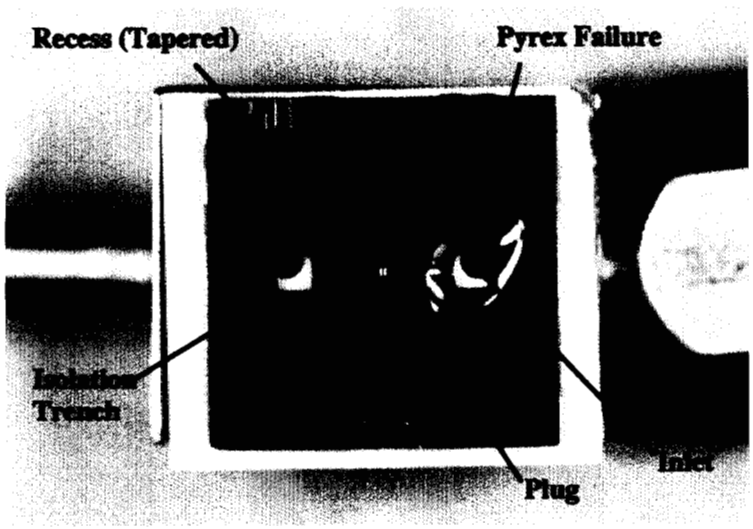


Fig. 12: Post-Test Image of Burst "Batch-2" Type Chip. Notice Hole in Pyrex over Inlet.

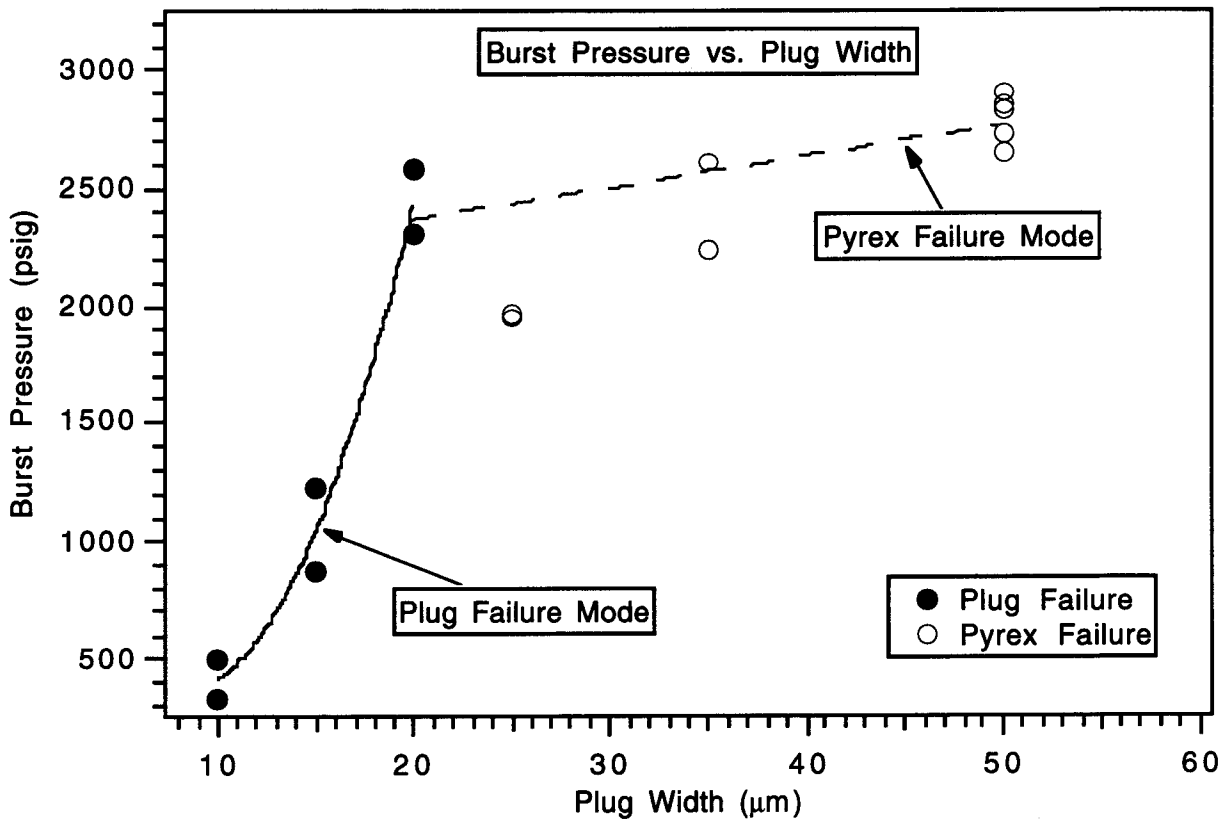


Fig. 13: Burst Pressure vs. Plug Width

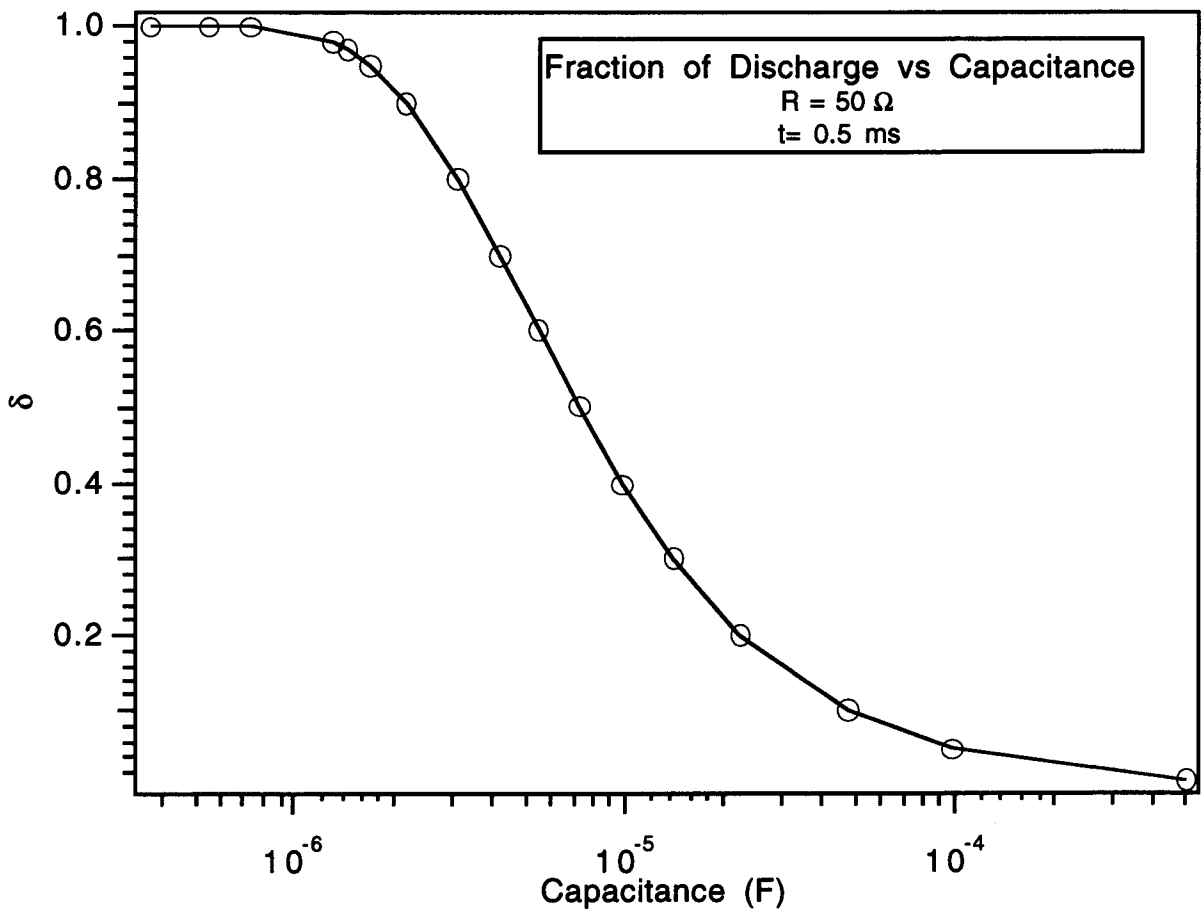


Fig. 14: Fraction of Discharge vs. Capacitance

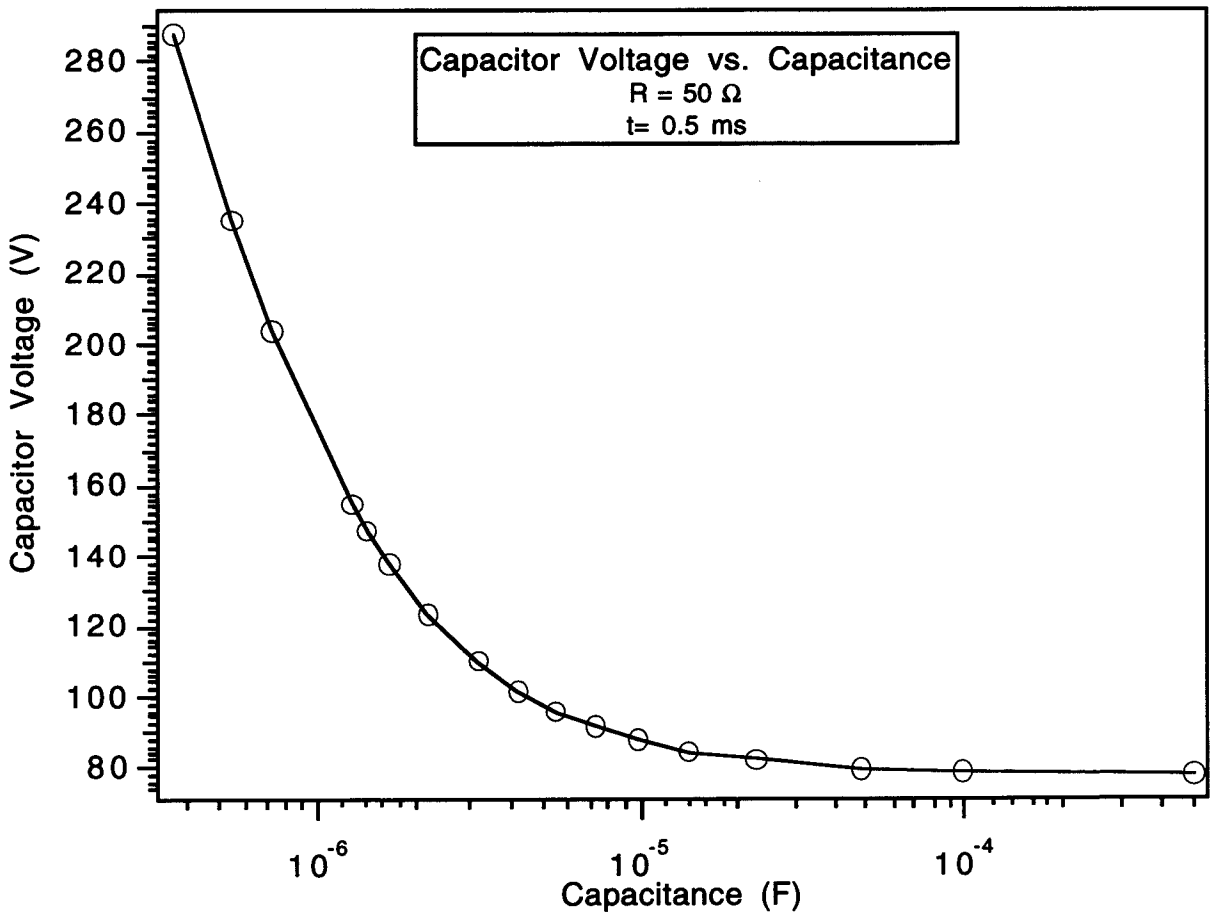


Fig. 15: Capacitor Voltage vs. Capacitance